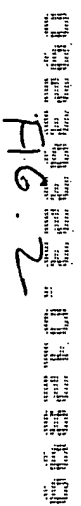
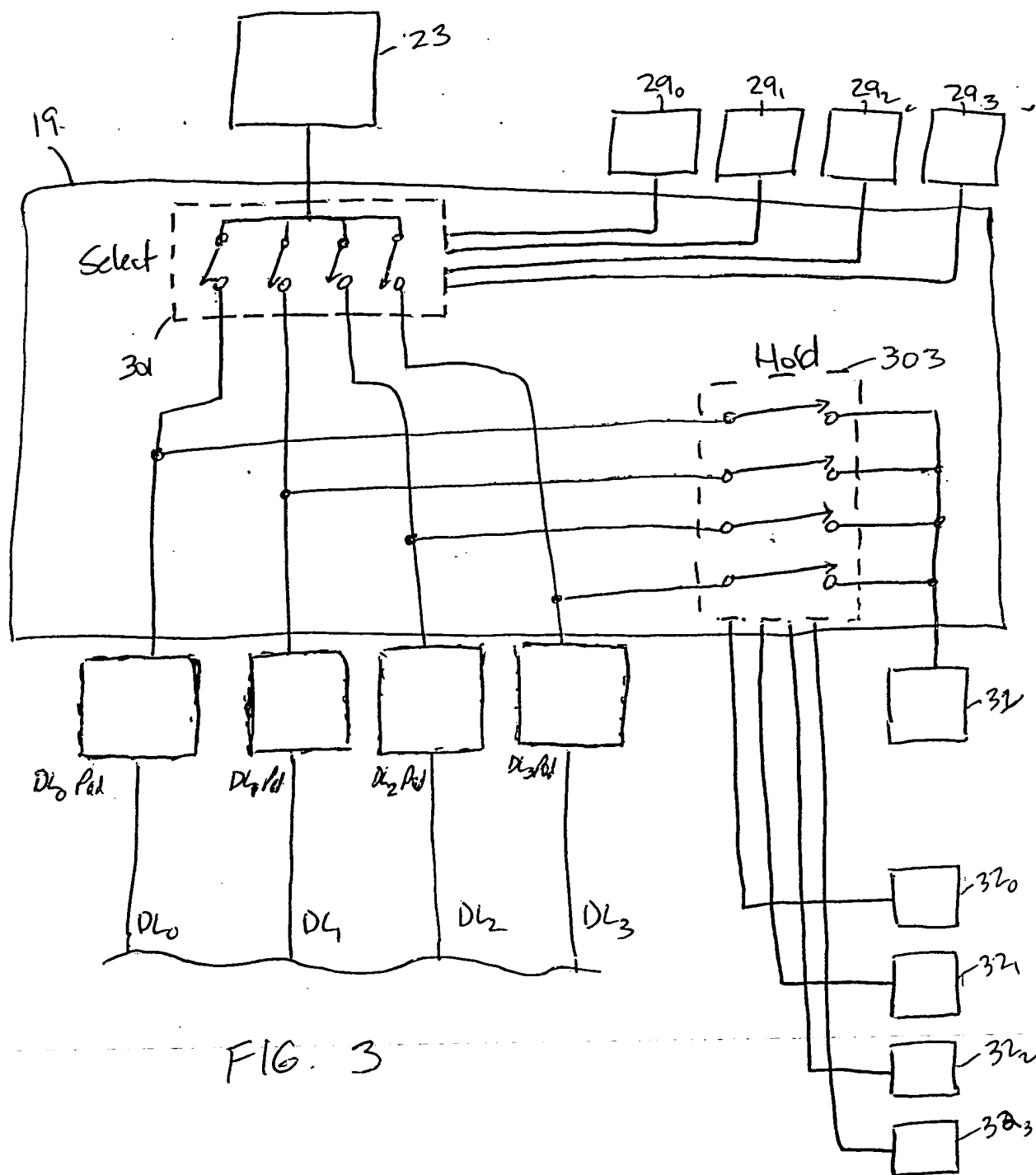
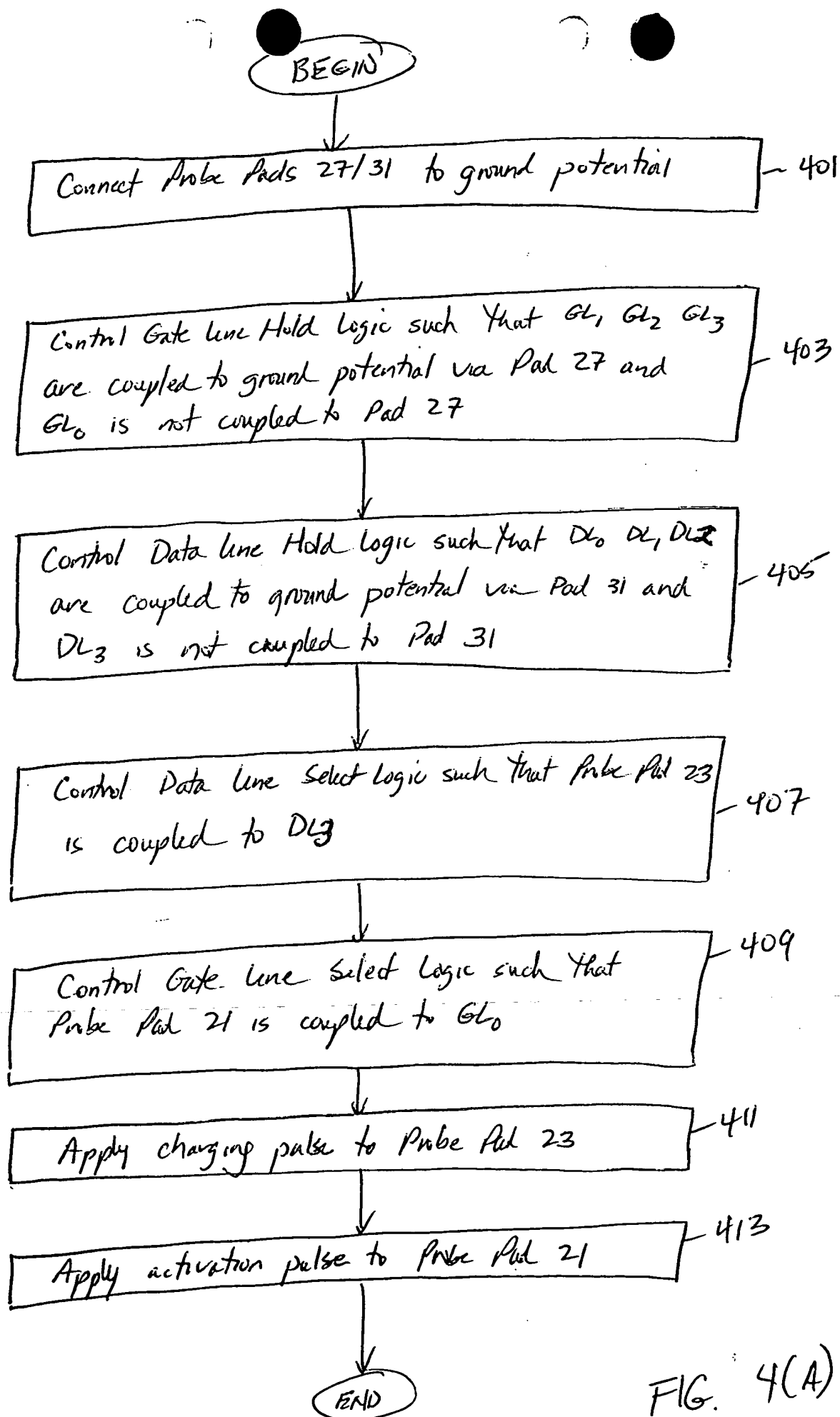


FIG. 1(B)



00000000000000000000





66270 666260

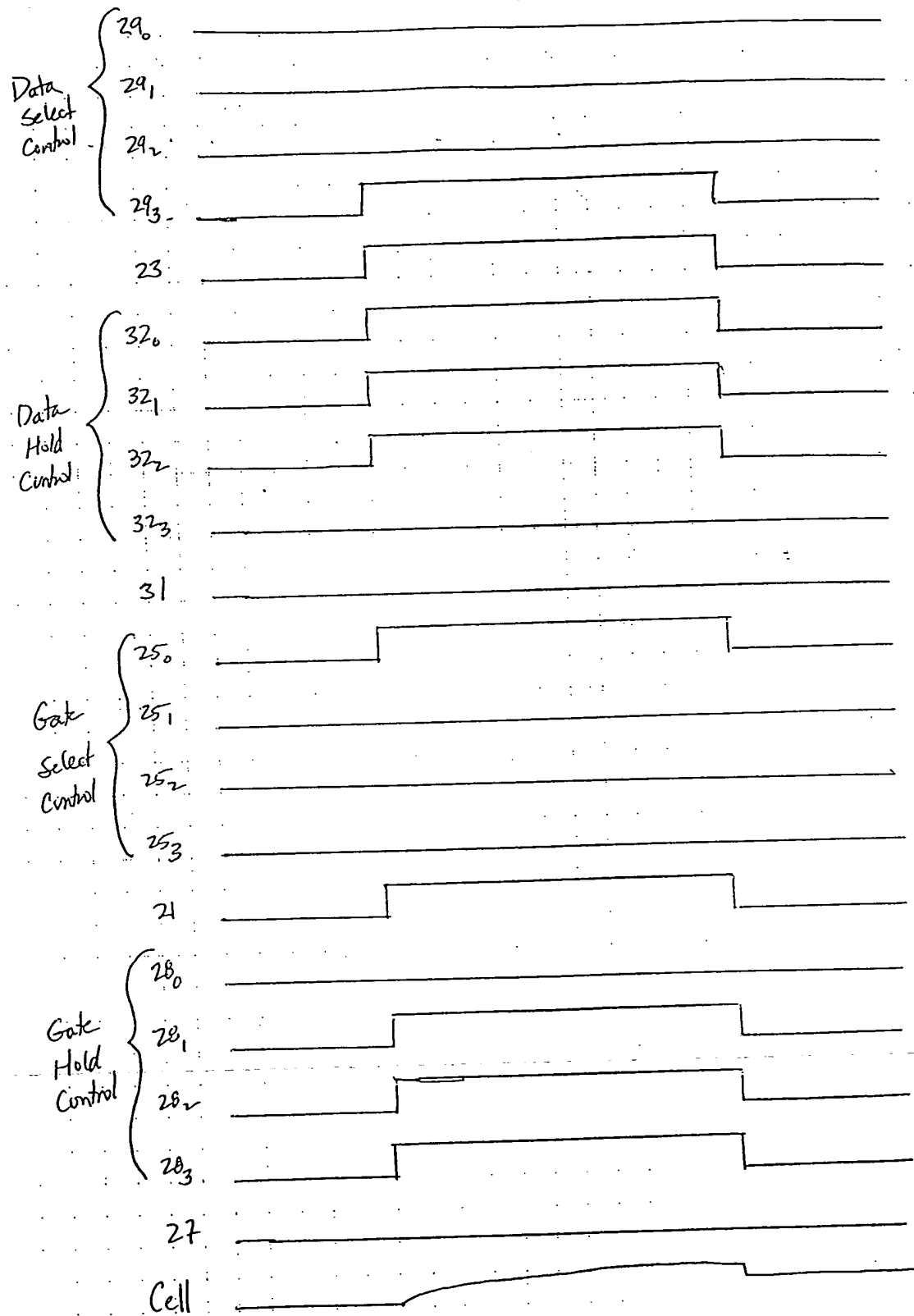


FIG. 4(B)

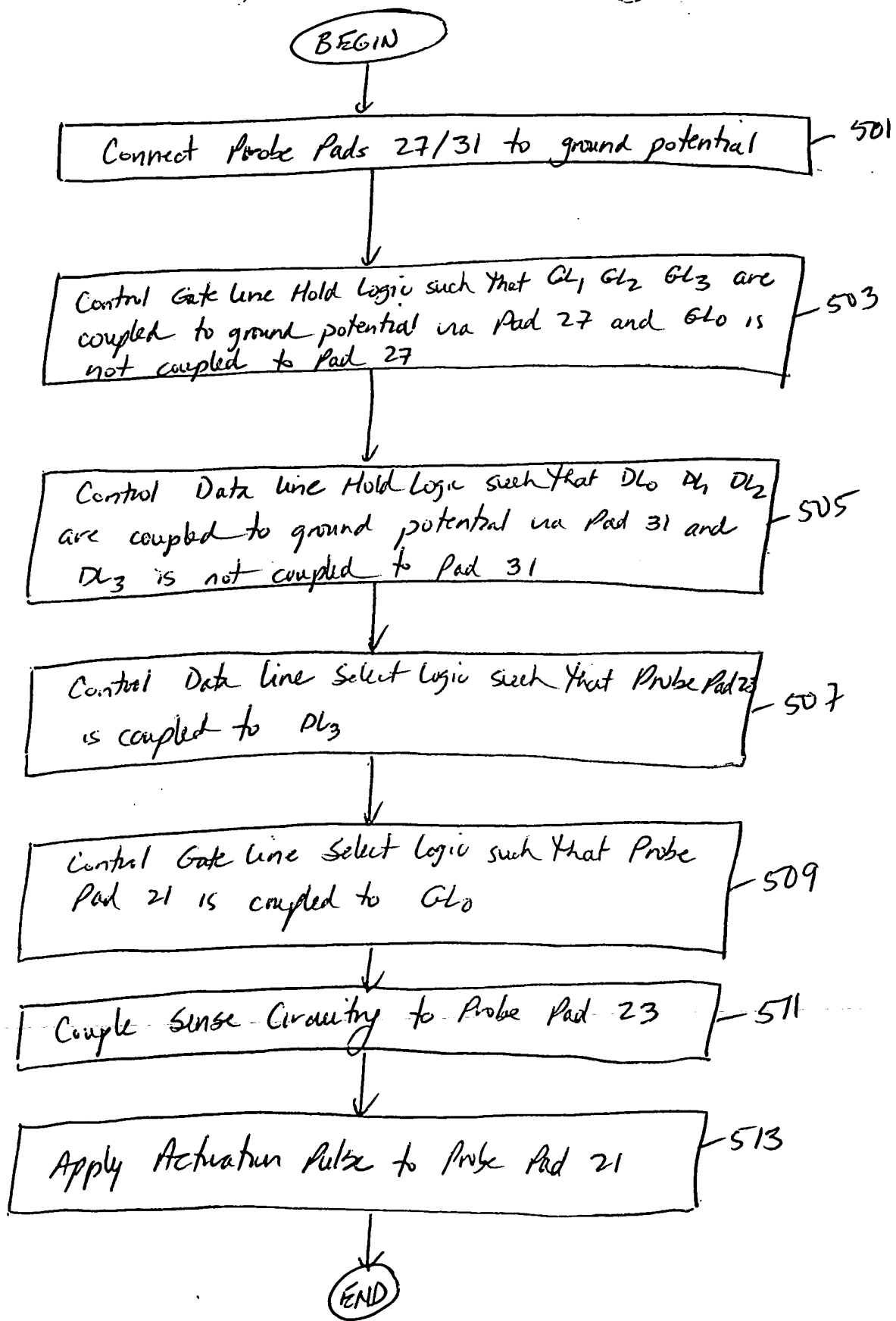


FIG. 5(A)

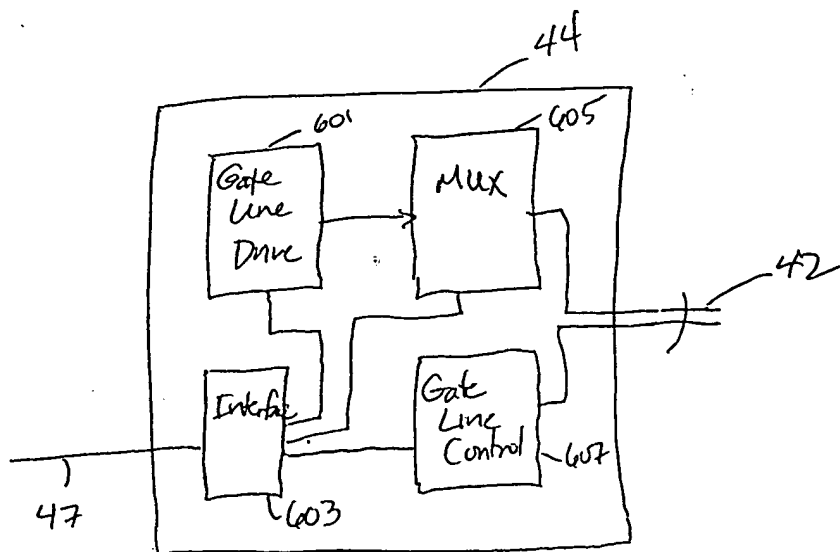
Timing diagram for the 74164 8-bit shift register. The diagram shows the relationship between Data Select Control (290-293), Data Hold Control (320-323), Gate Select Control (250-253), and Gate Hold Control (280-283) signals over time. The 293 signal is active high, while 290, 291, and 292 are active low. The 320, 321, and 322 signals are active high, while 323 is active low. The 250 signal is active high, while 251, 252, and 253 are active low. The 280, 281, and 282 signals are active high, while 283 is active low. The 27 signal is active high.

Wave form



FIG. 5(B)



[illegible]

F16. 6

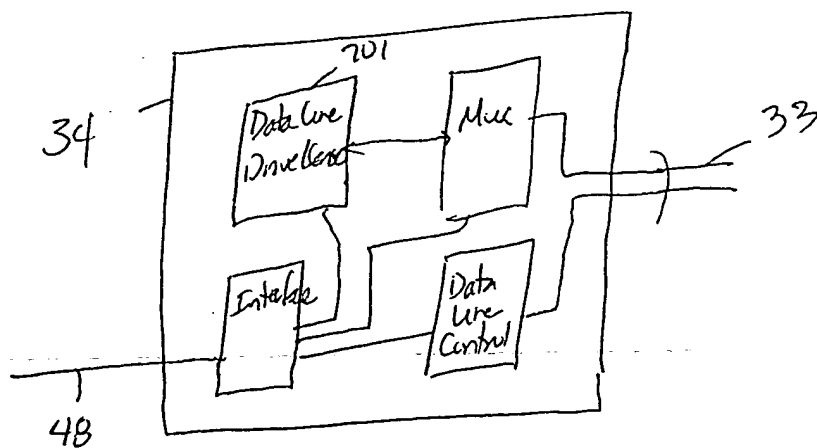


FIG. 7

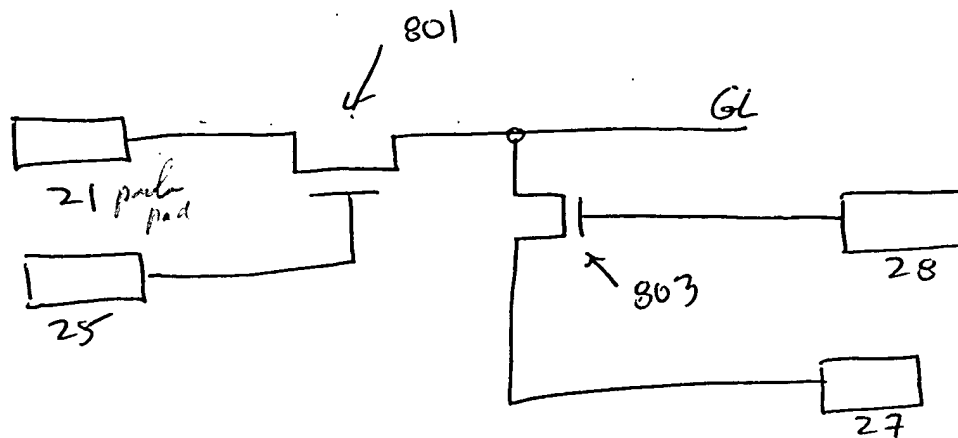


FIG. 8

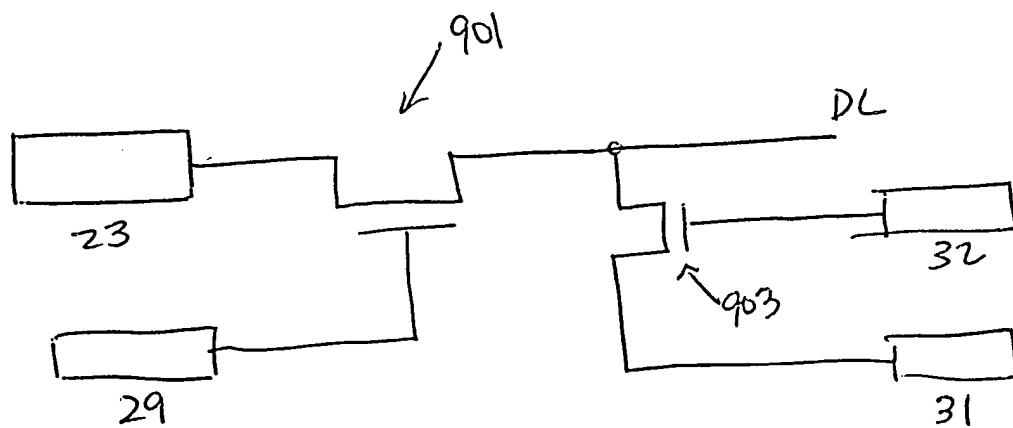


FIG. 9

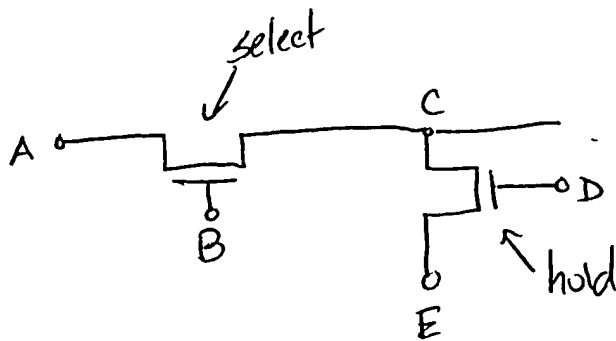


FIG. 10(A)

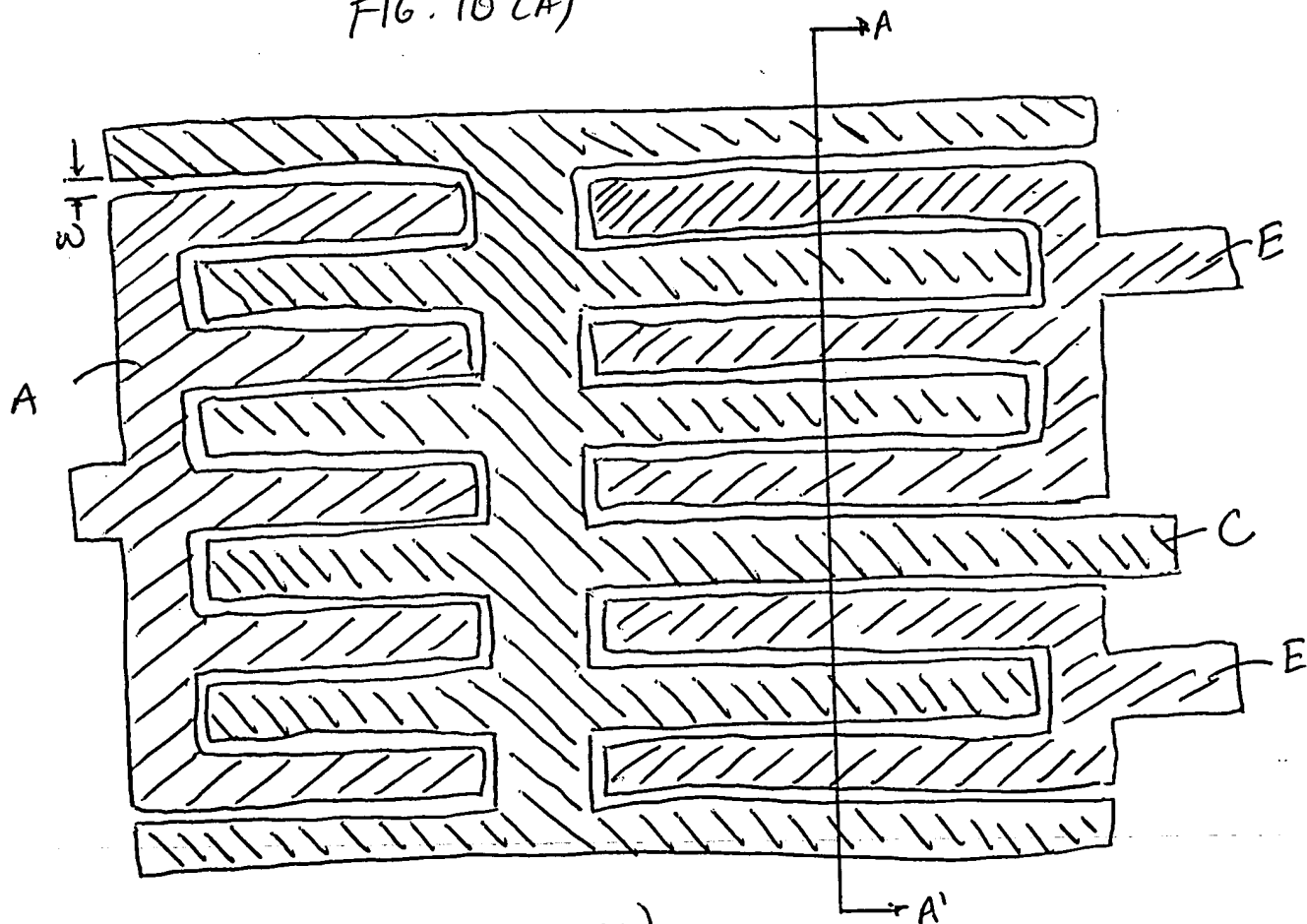


FIG. 10(B)

66321C(00)250

150

150

150

150

150

150

150